Communiqués de presse

La nouvelle puce IBM SyNAPSE pourrait ouvrir l'ère de vastes réseaux de neurones

- Inspirée du cerveau humain, la nouvelle puce comporte 1 million de neurones et 256 millions de synapses et rompt avec l'architecture de Von Neumann - Créée à partir de la technologie Samsung au procédé de 28nm, cette puce de 5,4 milliards de transistors entrelacés dispose d'une matrice de 4096 cœurs neurosynaptiques, tout en consommant seulement 70 mW pendant le fonctionnement en temps réel - Un écosystème complet de matériel et logiciels cognitifs repousse les limites de l'informatique mobile, du Cloud, du calcul intensif (HPC) et des systèmes embarqués

Paris - 25 août 2014: Les scientifiques d'IBM ont dévoilé aujourd'hui la première puce neurosynaptique comportant le nombre sans précédent de 1 million de neurones programmables, 256 millions de synapses programmables et 46 milliards d'opérations synaptiques par seconde et par watt. Pourvue de 5,4 milliards de transistors, cette puce entièrement fonctionnelle et qu'on peut fabriquer en quantité industrielle est actuellement l'une des plus grandes puces CMOS jamais construites. En mode d'exécution au rythme biologique, elle ne consomme que quelques 70mW, ce qui, en termes d'énergie, est proportionnellement moins important que ce que consomme un microprocesseur moderne. Ce supercalculateur neurosynaptique fait la taille d'un timbre de poste et consomme autant d'énergie que la batterie d'une prothèse auditive. Il s'agit là d'une technologie à même de transformer la science, l'ingénierie, les affaires, le gouvernement et la société par la création d'applications cognitives visuelles, auditives ou multi-sensorielles.

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New IBM SyNAPSE Chip Could Open Era of Vast Neural Networks

New chip with brain-inspired non-von Neumann computer architecture has one million neurons and 256 million synapses

Built on Samsung's 28nm process technology, the 5.4 billion transistors chip has an on-chip network of 4096 neurosynaptic cores but only consumes 70mW during real-time operation

Complete cognitive hardware and software ecosystem opens new computing frontier for mobile, cloud, supercomputing and distributed sensor applications

Scientists from IBM (NYSE: IBM) today unveiled the first neurosynaptic computer chip to achieve an unprecedented scale of one million programmable neurons, 256 million programmable synapses and 46 billion synaptic operations per second per watt. At 5.4 billion transistors, this fully functional and production-scale chip is currently one of the largest CMOS chips ever built, yet, while running at biological real time, it consumes a minuscule 70mW—orders of magnitude less power than a modern microprocessor. A neurosynaptic

supercomputer the size of a postage stamp that runs on the energy equivalent of a hearing-aid battery, this technology could transform science, technology, business, government, and society by enabling vision, audition, and multi-sensory applications.

Today's breakthrough, published in *Science* in collaboration with Cornell Tech, is a significant step towards bringing cognitive computers to society.

There is a huge disparity between the human brain's cognitive capability and ultra-low power consumption when compared to today's computers. To bridge the divide, IBM scientists created something that didn't previously exist—an entirely new neuroscience-inspired scalable and efficient computer architecture that breaks path with the prevailing von Neumann architecture used almost universally since 1946.

This second generation chip is the culmination of almost a decade of research and development, including the initial single core hardware prototype in 2011 and software ecosystem with a new programming language and chip simulator in 2013.

The new cognitive chip architecture has an on-chip two-dimensional mesh network of 4096 digital, distributed neurosynaptic cores, where each core module integrates memory, computation, and communication, and operates in an event-driven, parallel, and fault-tolerant fashion. To enable system scaling beyond single-chip boundaries, adjacent chips, when tiled, can seamlessly connect to each other—building a foundation for future neurosynaptic supercomputers. To demonstrate scalability, IBM also revealed a 16-chip system with sixteen million programmable neurons and four billion programmable synapses.

"IBM has broken new ground in the field of brain-inspired computers, in terms of a radically new architecture, unprecedented scale, unparalleled power/area/speed efficiency, boundless scalability, and innovative design techniques. We foresee new generations of information technology systems – that complement today's von Neumann machines – powered by an evolving ecosystem of systems, software, and services," said Dr. Dharmendra S. Modha, IBM Fellow and IBM Chief Scientist, Brain-Inspired Computing, IBM Research. "These brain-inspired chips could transform mobility, via sensory and intelligent applications that can fit in the palm of your hand but without the need for Wi-Fi. This achievement underscores IBM's leadership role at pivotal transformational moments in the history of computing via long-term investment in organic innovation."

The Defense Advanced Research Projects Agency (DARPA) has funded the project since 2008 with approximately $53M via Phase 0, Phase 1, Phase 2, and Phase 3 of the Systems of Neuromorphic Adaptive Plastic Scalable Electronics (SyNAPSE) program. Current collaborators include Cornell Tech and iniLabs, Ltd.

Building the Chip

The chip was fabricated using Samsung's 28nm process technology that has a dense on-chip memory and low-leakage transistors.

"It is an astonishing achievement to leverage a process traditionally used for commercially available, low-power mobile devices to deliver a chip that emulates the human brain by processing extreme amounts of sensory information with very little power," said Shawn Han, vice president of Foundry Marketing, Samsung Electronics.

“This is a huge architectural breakthrough that is essential as the industry moves toward the next-generation cloud and big-data processing. It’s a pleasure to be part of technical progress for next-generation through Samsung’s 28nm technology.”

The event-driven circuit elements of the chip used the asynchronous design methodology developed at Cornell Tech and refined with IBM since 2008.

“After years of collaboration with IBM, we are now a step closer to building a computer similar to our brain,” said Professor Rajit Manohar, Cornell Tech.

The combination of cutting-edge process technology, hybrid asynchronous-synchronous design methodology, and new architecture has led to a power density of 20mW/cm2 which is nearly four orders of magnitude less than today’s microprocessors.

Advancing the SyNAPSE Ecosystem

The new chip is a component of a complete end-to-end vertically integrated ecosystem spanning a chip simulator, neuroscience data, supercomputing, neuron specification, programming paradigm, algorithms and applications, and prototype design models. The ecosystem supports all aspects of the programming cycle from design through development, debugging, and deployment.

To bring forth this fundamentally different technological capability to society, IBM has designed a novel teaching curriculum for universities, customers, partners, and IBM employees.

Applications and Vision

This ecosystem signals a shift in moving computation closer to the data, taking in vastly varied kinds of sensory data, analyzing and integrating real-time information in a context-dependent way, and dealing with the ambiguity found in complex, real-world environments.

Looking to the future, IBM is working on integrating multi-sensory neurosynaptic processing into mobile devices constrained by power, volume and speed; integrating novel event-driven sensors with the chip; real-time multimedia cloud services accelerated by neurosynaptic systems; and neurosynaptic supercomputers by tiling multiple chips on a board, creating systems that would eventually scale to one hundred trillion synapses and beyond.

Building on previously demonstrated neurosynaptic cores with on-chip, online learning, IBM envisions building learning systems that adapt in real world settings. While today’s hardware is fabricated using a modern CMOS process, the underlying architecture is poised to exploit advances in future memory, 3D integration, logic, and sensor technologies to deliver even lower power, denser package, and faster speed.

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